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Neutral Point Voltage Balancing in Three Level Neutral Point Clamped (NPC) Multilevel Inverter Using Carrier Based Offset Addition PWM

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Abstract: Three-level Neutral Point Clamped (NPC) converters are widely applied in high power medium voltage electrical drive systems. A significant problem related to the three-level NPC converters is the fluctuation of the neutral-point voltage. In this paper, a neutral point voltage balancing technique is proposed that injects an offset voltage into the sinusoidal modulating signals of the conventional Carrier-Based Pulse Width Modulation (CBPWM) method. Furthermore, when the injected offset voltage is maximized, it is not only balance the dc-link capacitors voltages, but also reduce output voltage distortions and switching losses. And also, the CBPWM offset addition method has reduced the switching commutations number to the lesser values. The performances of the strategies were verified by simulation tests. Modulation (PWM) strategies developed with continuous offset addition is demonstrated by MATLAB/SIMULINK based simulation presented in this paper.

Keywords: NPC inverter; 3 phase induction motor; offset addition;diode clamped inverter; multilevel inverter; carrier based PWM; dq theory; pi control.

I. INTRODUCTION

Neutral Point Clamped (NPC) multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium voltage energy control. The structure of diode clamped inverters allows them to reach high voltages and therefore lower voltage rating devices can be used. As the number of levels increases the output waveform with more steps producing a very fine stair case wave and approaching very closely to the desired sinusoidal wave.

Hence Neutral point clamped multilevel inverters offer a better choice at a high power end because the high volt-ampere ratings are possible with these inverters without the problems of high dv/dt and the other associated ones.

NPC inverter has an inherent problem of unbalanced voltages across dc-link capacitors due to load unbalancing, non uniform distribution of charges in the capacitors, and non-identical properties of dc-link capacitors provided from the manufacturer [1], [2]. Several open loop strategies have been proposed for the reduction of the harmonic content [3], [4].

The authors have proposed two ways of mid-point voltage balancing in three level NPC inverters. One way of voltage balancing based upon the addition or modification of hardware circuitry to the inverter [5]-[10] which modify the charging and discharging currents of DC-link capacitors. Second way of voltage balancing is based upon modification in inverter control strategy based on PWM schemes. Many carrier and SVPWM based strategies have been proposed for the modulation of theses inverters [11]-[15].

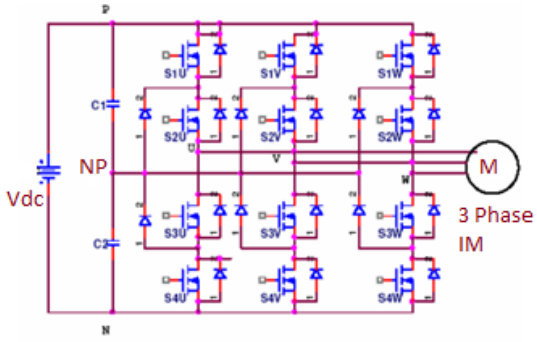

Fig.1. Three phase three-level NPC

S_{1U}	S_{2U}	S_{3U}	S_{4U}	Switching states	Voltage output(V_{uo})
1	1	0	0	P	$+V_{dc}/2$
0	1	1	0	0	0
0	0	1	1	N	$-V_{dc}/2$

Table 1: Switching states of three level NPC inverter

A closed loop control strategy, which reduces the harmonic content as well as maintains voltage stability in the neutral point is presented in this paper. Closed loop regulator is based on injecting offset magnitude to the modulating signal as a function of a control input that corrects any existing imbalance.

In this paper main considerations given to regulate the voltage imbalance of NPC inverter employing sine-triangle modulator in conjunction with a closed-loop controller, which considerably reduces the harmonic distortions in the output voltage waveform, resulting in reduction of the required dc bus capacitance.

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II. NEED OF NEUTRAL POINT BALANCING

The Neutral point clamped inverter is showed in Fig.1 and Table I give the switching states to generate the three level output voltage for phase U.

Due to unequal voltages across two dc-link capacitors PWM inverter output voltage and output current waveforms get distorted. Unbalance DC link creates increased voltage stress on switching devices. Increased voltage imbalance across dc-link capacitors may cause failure of devices. Therefore, Neutral point voltage balancing control is necessary without sacrificing the harmonic performance of the inverter. Fig. 2(a) and (b) shows the waveforms and harmonic spectrums of phase voltage and line voltage under burst condition of large imbalance at dc link with Vdc1 = 200 V and Vdc2 = 400 V. Under this condition, the dc component and even-order harmonics are more significant which are dangerous for drive and other applications.

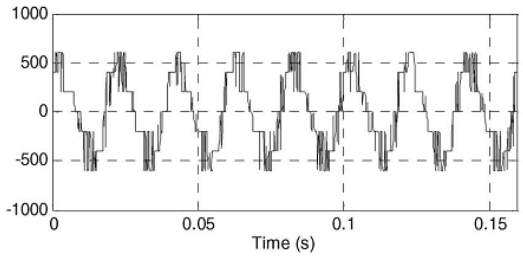

Fig. 2 Output line voltage distortions due to unbalanced DC-link voltage

III. DESIGN OF CLOSED LOOP NPC INVERTER

Design of closed loop NPC inverter consider the following important aspects,

a) Ensure dc-link capacitor, voltage balancing and regulating dc-link voltage
b) Minimization of inverter voltage harmonics and current harmonics
c) Ensuring less and uniform switching stress on switching devices, resulting in reduced switching losses.

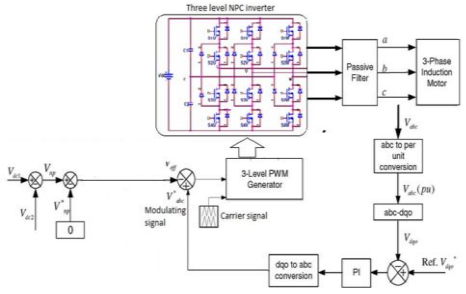

Fig.3 NPC offset addition PWM block diagram

Fig. 3 shows the complete block diagram of the NPC offset addition PWM. It consists of both a dc-link voltage control loop and a load voltage control loop. Three phase load voltages are sensed and converted into a per-unit quantity. These per-unit voltages abc-axis are converted into dqo-axis. After comparing with preset values (V_d=1,V_q=0) again converted to abc-signal. This Vabc signal is added with the dc-link voltage control loop generated offset signal. This signal is acting as modulating signal. It is compared with triangle carrier PWM by using level shifted PWM and the pulses are given to appropriate switches.

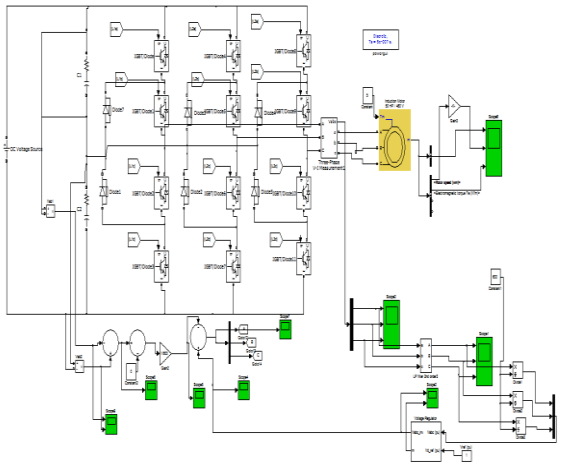

Fig.4 abc to dqo conversion reference comparison and dqo to abc conversion

Fig.4 shows the measured voltage Vabc is converted by using the abc to dqo conversion method using the following three-phase to two-phase conversion:

V_d = 2/3[Va sin(ωt)+Vb sin(ωt − 120°)+Vc sin(ωt − 240°)] V_q=2/3[Va cos(ωt)+Vb cos(ωt −120°)+Vc cos(ωt − 240°)] V_o=Va+ Vb +Vc

These dqo voltages (V_{dqo}) are compared with preset values of dqo voltages (V^*_{dqo}). It results in voltage error which is processed through a PI controller to generate two axis command signals V^*_{dqo}. Then, three-phase reference voltage signals are ynthesized using the following two-phase to three-phase conversion:

V_a= V_d sin(ωt) + V_q cos(ωt) + V_o)
V_b = V_d sin(ωt − 1200) + V_q cos(ωt − 1200) + V_o)
V_c = V_d sin(ωt − 2400) + V_q cos(ωt − 2400) + V_o)

These are the reference sinusoidal modulating signal V_{abc}*. The amplitude modulation index m is defined as

$$m = \sqrt{V_d^2 + V_q^2}$$

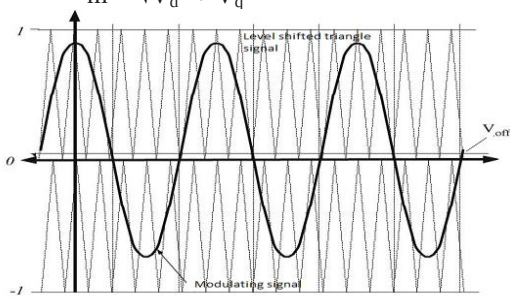

Fig.5 Offset addition PWM

offset addition method is shown in Fig.5 to the reference sinusoidal signal. The compared signal is given to switches as sequence in the corresponding phase legs

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IV. SIMULATION RESULTS

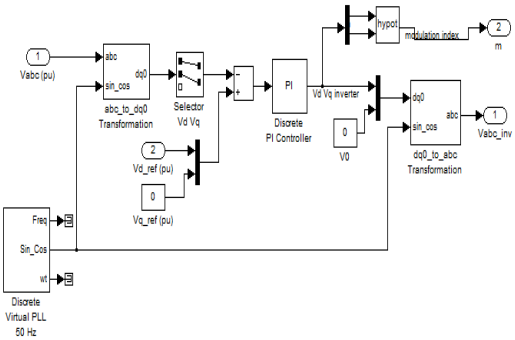

Fig.6 A MATLAB/Simulink model of three-phase three-level NPC MLI based 3 phase induction motor with the carrier-based offset addition PWM

MATLAB/Simulink model of three-phase three-level DCMLI with the carrier-based offset addition PWM is shown in fig.6

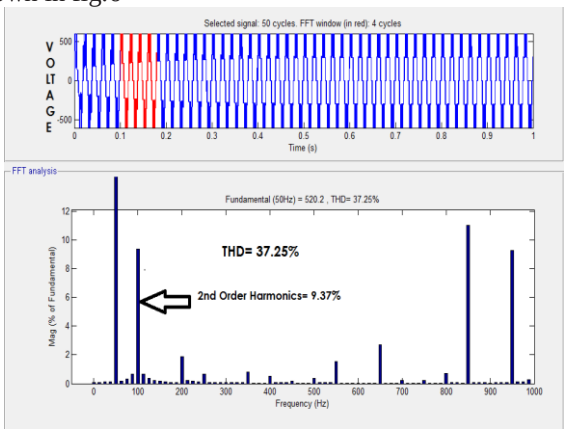

Fig.7 Simulated inverter line voltage (Vab) and its frequency spectrum with unbalanced dc link without closed loop offset PWM

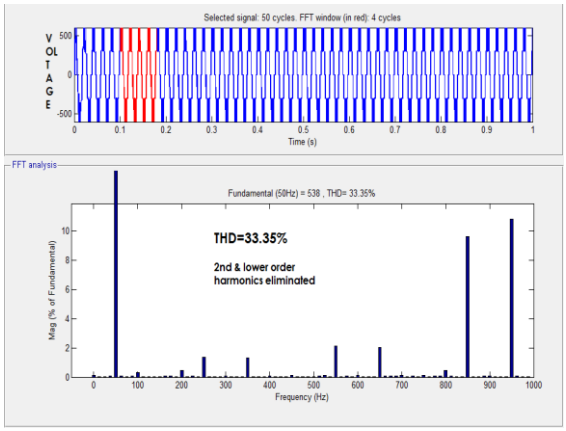

Fig.8 Simulated inverter line voltage (Vab) and its frequency spectrum with unbalanced dc link with Neutral point balancing.

Frequency spectrum of output line voltage without closed loop offset PWM are shown in Fig. 7 with fundamental value as 520.2 and 37.25 % of THD. In Fig.8 frequency spectrum for closed loop NPC inverter with offset addition PWM is shown with fundamenatal value as 538 V and THD values as 33.35%

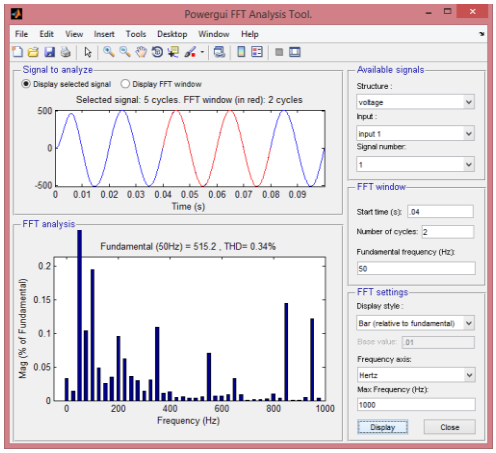

Fig.9 Simulated inverter line voltage (Vab) and its frequency spectrum with unbalanced dc link with neutral point balancing after filtering.

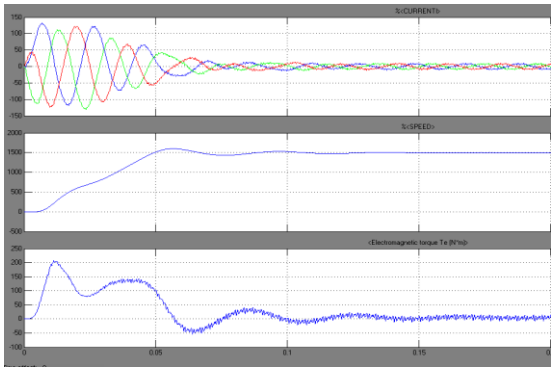

Fig.10 Stator current waveform (Ia, Ib and Ic) , Motor speed (rpm), Electromagnetic torque waveforms under balanced dc link voltages after neutral point voltge balancing.

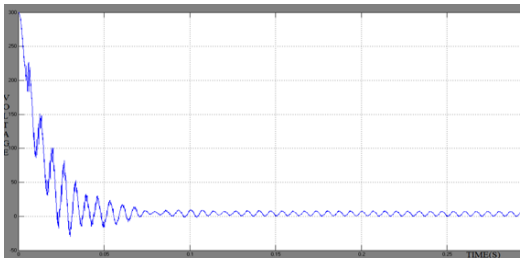

Fig.11 Neutral point voltage (Vnp= Vdc1-Vdc2)

V. CONCLUSION

A simple carrier-based neutral voltage balancing for a three-level Neutral Point Clamped (NPC) Multilevel inverter in conjunction with a closed-loop controller has been proposed in this paper. The proposed offset calculation PWM gives improved inverter performance in terms of reduced THD,with unbalanced dc-link voltages,improved neutral point voltage harmonic profile, and balanced dc link with almost zero average Neutral point potential.

The proposed method is in the determination of the magnitude of variable offset voltagebasedupon the average value, peak-to-peak amplitude,THD's and third harmonic content in neutral point voltage.This not only regulates the neutral point voltage but also reduces the harmonic

contents in inverter output voltages and currents. Simultaneously fundamental output voltage and second-order harmonics in inverter output voltage get eliminated which may otherwise produce torque pulsations, harmonic currents, and additional power losses. Aside from maintaining the dc-bus voltage balance, the proposed closed loop offeset voltage PWM leads to a significant reduction in the voltage distortion.

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